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Attorney's Docket No.: 07977-093002 / US3164D1

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant : Hisashi Ohtani, et al. Art Unit : 2815
Serial No. : 09/379,702 Examiner : Eugene Lee
Filed : August 24, 1999
Title : METHOD OF FABRICATING SEMICONDUCTOR DEVICES

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

REPLY TO ACTION OF AUGUST 19, 2003

In reply to the Office Action of August 19, 2003, Applicant submits the following remarks.

Claims 45-64 are pending in this application, with claims 45-50 being independent.

The claims have been rejected as being obvious over Yamazaki in view of Matsumoto. Recognizing that Yamazaki does not disclose a gate insulating film comprising a first insulating film and a second insulating film extending beyond an edge of the first insulating film, the Examiner asserts that Matsumoto describes a thin film transistor 2 that has a second gate insulating film 19 that extends all the way across the semiconductor device, and that it would have been obvious to include Matsumoto's gate insulating film in Yamazaki's device in order to increase the on-voltage and suppress the increase in current consumption.

Applicant requests reconsideration and withdrawal of this rejection because, absent impermissible hindsight reconstruction of the invention, one of ordinary skill in the art would have had no motivation to combine the references in the manner suggested by the Examiner.

Yamazaki describes an insulated gate field effect transistor in which a gate insulating layer 3 having the same dimensions as a semiconductor layer 2 is formed by forming an insulating layer 3' on a semiconductor layer 2' and etching the insulating layer 3' and the semiconductor layer 2' to form the insulating layer 3 and the semiconductor layer 2. A gate electrode 5G then is formed on the insulating layer 3.

Matsumoto describes a circuit in which a gate insulating film 14 is formed over the entire surface of an insulating substrate 1 that includes a polysilicon thin film 11 corresponding to a transistor 2 of a matrix circuit and polysilicon thin films 12 and 13 corresponding to transistors 4

and 5 of a peripheral circuit. Gate electrodes 15 and 16 are formed on the film 14 in regions corresponding to the thin films 12 and 13. Thereafter, an interlayer insulating film 19 is formed over the entire surface of the gate insulating film 14. Finally, a gate electrode 20 is formed on the film 19 in a region corresponding to the thin film 11. Thus, Matsumoto describes forming a matrix circuit having a transistor 2 in which the gate electrode 20 is separated from the thin film 11 by two insulating films that extend over the entire substrate 1, and a peripheral circuit having transistors 4 and 5 in which the gate electrodes 15 and 16 are separated from the thin films 12 and 13 by a single insulating film that extends over the entire substrate 1. Matsumoto notes, at col. 5, line 20, that the added thickness provided by the two insulating films causes the transistor 2 of the matrix circuit to have a higher on-voltage and a broader range of off-voltages than the transistor 4 of the peripheral circuit.

Yamazaki is unclear as to whether the transistor is for use in a peripheral circuit or a matrix circuit. To the extent that the transistor is being used in a peripheral circuit, nothing in Matsumoto would have led one of ordinary skill in the art to add a second insulating film before forming the gate electrode, since Matsumoto employs only a single insulating film under the gate. To the extent that the transistor is being used in a matrix circuit, Matsumoto merely indicates that performance characteristics of the matrix transistors may be modified by using a thicker gate insulating film. However, as such a thicker insulating film could be obtained by making insulating layer 3 thicker in the first instance, rather than by employing the additional process step of applying a second insulating film, this teaching by Matsumoto would not have led one of ordinary skill in the art to employ a second insulating film.

For at least these reasons, applicant requests reconsideration and withdrawal of the rejection of claims 45-64. Moreover, in the prior response, applicant requested reconsideration and withdrawal of this rejection for similar reasons. In particular, applicant noted that neither Yamazaki, Matsumoto, nor any combination of the two describes or suggests a gate insulating film including a first insulating film over a crystalline semiconductor island and a second insulating film over the first insulating film, with the first insulating film having a side aligned with a side of the crystalline semiconductor island and the second insulating film extending

beyond an edge of the first insulating film, as recited in each of the independent claims. The current action responds to these arguments by noting that they are moot in view of the new grounds of rejection. However, the action includes no new ground of rejection. In the event that the Examiner decides to maintain this rejection, applicant requests a substantive response to the applicant's argument, and applicant further suggests that a final rejection would be improper since the applicant has not had an opportunity to address any concerns that the Examiner may have regarding the arguments raised in the prior response, since those concerns, if present, were not expressed in the current action.

Applicant submits that all claims are in condition for allowance. Please apply any charges or credits to deposit account 06-1050.

Respectfully submitted,

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